INVERTER MATRIX FOR THE CLEMENTINE MISSION

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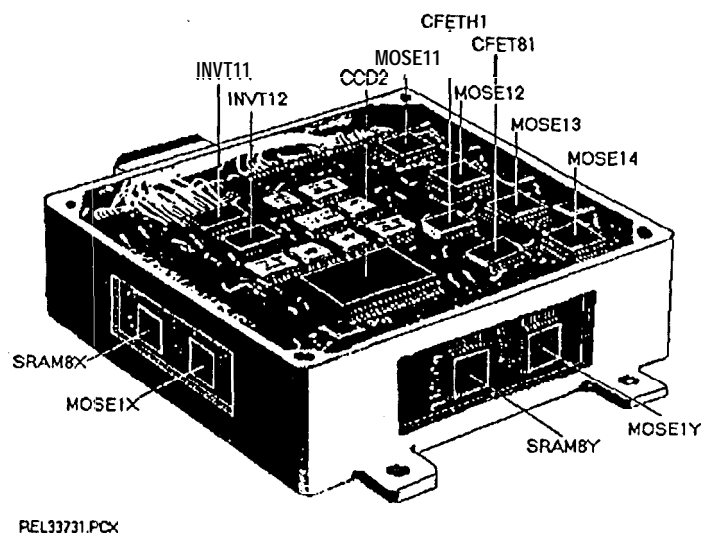California Institute of Technology
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ABSTRACT

An **inverter** matrix test circuit was designed for the **Clementine** space mission and is built into the RRELAX (Radiation and Reliability Assurance Experiment). The objective is to develop a circuit that will allow the evaluation of the CMOS FETs using a lean data set in the noisy spacecraft environment. As will be shown, only nine data points are needed to acquire ten CMOS FET parameters.

INTRODUCTION

An inverter matrix was designed for the RRELAX and included on the **Clementine** space mission. Two **RRELAX** units were fabricated. One unit is included on the **Clementine** spacecraft which will orbit the moon and fly-by the asteroid **Geographos.** The second unit is included on the Inter-Stage Adaptor (ISA) which goes into a **translunar** orbit. The **Clementine** is scheduled for launch on January 25, 1994.

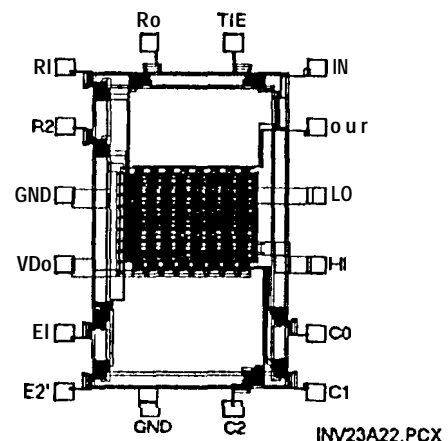The RRELAX, shown in Fig. 1, is by 4" x 4" x 1.5", weighs 22 oz and requires 2.5 watts peak power.

The unit contains an 80C86 microprocessor operating at 2.4 MHz and data acquisition **circuitry** to measure the experimental devices. The **data** is stored in the RRELAX memory and the results sent to the spacecraft through a serial port for **down-linking.**

The labels in Fig. 1 point to the experimental devices including **SRAMs** for Cosmic Ray detection, **p-FETs** for total dose measurement, and a CCD for radiation effects analysis. The locations of the two inverter matrices are shown in the figure. One matrix has a 7-roil Al equivalent shield and the other a **37-mil** Al equivalent shield.

The inverter matrix was developed to evaluate CMOS FETs fabricated at a rad-soft rapid-prototype CMOS foundry in order to evaluate its space worthiness. The FETs included in the inverter matrix are typical of FETs found in integrated circuits. In addition the matrix was designed to require a small data set in order to minimize spacecraft down-link capacity. As **will** be shown, only nine data points are needed to characterize ten **n-** and **p-FET** parameters.

The layout of the **inverter** matrix, shown in Fig. **2,** is similar to the inverter matrix developed in the

REL33731.PCX

Figure 1. RRELAX showing the arrangement of test devices. The **inverter** matrices are labeled **INVT11** (208) **and INVT12** (207).

INV23A22.PCX

Figure 2. **Inverter** matrix with 64 test **inverters** arranged in four identical quadrants. The chip size is 1.63 x 2.58 mm^2.

'middle 80's for evaluating process statistics [1] and [2]. The matrix consists of 64 inverters arranged in four identical quadrants. In two of the quadrants, the gates are biased high during radiation and in the other two quadrants, the gates are biased low during irradiation. The dimensions of the inverter matrix FETs are listed in Table 1.

The key to this approach is the dependence of the inverter threshold voltage, VTi, on geometry [3]:

$$(1) \quad VTi = \frac{VDD + VT_n\sqrt{\beta_r} - VT_p}{1 + \sqrt{\beta_r}}$$

where VT_n is the n-FET threshold voltage, and VT_p is the magnitude of the p-FET threshold voltage. The dependence of VT_i on geometry, shown in Fig. 3, indicates how VTi depends on the geometry of the inverter, β_r:

$$(2) \quad \beta_r = \frac{\beta_n}{\beta_p} = \frac{KP_n (W_n - \Delta W_n)(L_p - ALP)}{KP_p (W_p - \Delta W_p)(L_n - AL_n)}$$

where KP $= \mu_0 \cdot C_0$; μ_0 is the zero-field channel mobility and Co is the gate capacitance per unit area. The FET design width is W, and L is the design length. The actual width and length are described using ΔW and AL. Notice that for $\beta_r \rightarrow 0$, VTi $\approx$ VDD - VT_p and for $\beta_r \rightarrow \infty$, VTi = VT_n.

The transfer curves for the 16 inverters listed in Table 1 are shown in Fig. 4. The inverter threshold voltage is located at the intersection of transfer curve and the positive sloping Vout-Vin line.

FET MODEL

The analysis uses the fact that at the inverter threshold both n- and p-FETs are in saturation. Thus the following simple square-law drain-current expression adequately describes the n-FET behavior [4]:

$$(3) \quad ID_n = \frac{\beta_n(VT_i - VT_n)^2}{2[1 + \theta_n(VT_i - VT_n)]}$$

where

$$(4) \quad \beta_n = KP_n(W_n - \Delta W_n)/(L_n - AL_n)$$

and

$$(5) \quad \theta_n = \theta L_n/(L_n - AL_n)$$

The p-FET equations are:

$$(6) \quad ID_p = \frac{\beta_p(VDD - VTi - VT_p)^2}{2[1 + \theta_p(VDD - VTi - VT_p)]}$$

where

$$(7) \quad \beta_p = KPP(WP - \Delta W_p)/(L_p - ALP)$$

and

$$(8) \quad \theta_p = \theta L_p/(L_p - ALP)$$

The above FET models were chosen after numerous alternative models were tried. It was found that giving VT a spatial description lead to unstable solutions. This is understandable since the data points, as seen in Fig. 5, are not located near the VT extraction points. Also θ is described by an L-dependence only. When the offset term, θ_0, was introduced into the model, θ parameters were too unstable and fluctuated about zero. When θW was introduced into the model, these values also fluctuated about zero. The net result is a simple model that fits the data reasonably well and extracts reasonable parameters. Also the extraction procedure that is robust.

DATA FITTING PROCESS

The above equations were combined into the following equation set and fitted to the data shown in Fig. 5. The FET geometries for the cardinal points shown in Fig. 5 are given in Table 3. The equations for the n-FETs are:

$$(9) \quad \sqrt{I_n} = a_0 + a_1 \cdot VT_i + a_2 \cdot \frac{(VT_i - VT_n)^2}{(L_n - \Delta L_n)}$$

where

$$(10) \quad I_n = 2 \cdot ID_n(L_n - \Delta L_n)/(W_n - \Delta W_n)$$
$$(11) \quad a_0 = -VT_n \cdot \sqrt{KP_n}$$
$$(12) \quad a_1 = \sqrt{KP_n}$$
$$(13) \quad a_2 = -\theta L_n \cdot \sqrt{KP_n}/2$$

Using the above "a" coefficients, the n-FET parameters are:

$$(14) \quad VT_n = -a_0/a_1$$

$$(15) \quad KP_n = a_1^2$$
$$(16) \quad \theta L_n = -2a_2/a_1$$

The above equations are plotted as curves #4, #5, and #6 in Fig. 5.

The equations for the p-FETs are:

$$(17) \quad \sqrt{I_p} = b_0 + b_1 \cdot VT_i + b_2 \cdot \frac{(VDD - VT_i - VT_p)^2}{(L_p - DL_p)}$$

where

$$(18) \quad I_p = 2 \cdot ID_p(L_p - DL_p)/(W_p - DW_p)$$
$$(19) \quad b_0 = VT_p \cdot \sqrt{KP_p}$$
$$(20) \quad b_1 = -\sqrt{KP_p}$$
$$(21) \quad b_2 = -\theta L_p \cdot \sqrt{KP_p}/2$$

"Using the above "b" coefficients, the p-FET parameters are:

(22) $VT_P = VDD + a_0/a_1$

(23) $KP_p = a_1^2$
(24) $\theta L_p = 2a_2/a_1$

The p-FET curves are plotted as curves #1, #2, and #3 in Fig. 5.

The solution for the FET parameters, VT KP, and θL were obtained by using a least squares fitting procedure to determine the "a" and "b" coefficients of the linear equations, Eqs. 9 and 17. The least squares procedure was. embedded inside a Simplex solver. The Solver changed DL, DW, and VT in order to optimize the least squares coefficient of determination with the constraint that the estimated VT value equals the least squares VT value within a precision of 0.01.

The fit of the data to the cardinal points is shown by the curves given in Fig. 5. The fit is reasonable considering the simplicity of the FET model given in Eqs. 9 and 17. By design, the curves converge to a single value of VT_n and VT_P. The matrix contained additional FET geometries and so these were included in the analysis as "bonus" points which help stabilize the extraction of VT_n. As will be shown, VT_P has considerable variability because the data points are far from the VT_P extraction point.

The test results for the data plotted in Fig. 5 is listed in Table 2. The listing indicates that 5 p-FET and 5 n-FET parameters have been extracted from the data. The RRELAX extracted results are compared to results published by MOSIS. The RRELAX results are surprisingly close to the MOSIS results. The discrepancies can be explained by differences in extraction procedures and wafer-to-wafer parameter variations. The MOSIS parameter extraction occurs in the FET linear region; whereas, RRELAX parameter extraction occurs in the FET saturation region.

CIRCUIT DESCRIPTION

The inverter matrix, shown in Fig. 6, consists of an 8-by-8 array of test inverters fabricated in a 1.2-urn n-well CMOS process. The chip has enables, EI and E2', that allow two or more chips to be bussed together; power, VDD (5V) and ground, GND for decoder logic; row address, RO - R2 and column address CO - C2 for selecting the test inverter; test inverter power, HI, ground, LO, input, IN, and output, OUT; and logic input, TIE, that tristates IN and connects OUT to the addressed test inverter input. The 64 test inverters are arranged in 4 identical quadrants. The quadrants contain 16 test inverters having unique n- and p-FET geometries listed in Table 1. When the chip is deselected EI

and/or E2' inactive), the inverter inputs are biased low (0 V) in QUAD#1 and QUAD#3 and high (5 V) in QUAD#2 and QUAD#4.

The inverter matrix circuit diagram in Fig. 6 shows one test inverter (MN1 and MP1) and supporting select transistors. The dashed lines indicate connections to the remaining seven rows and seven columns of the matrix. Row and column decoders are used to select one of the 64 test inverters for measurement. These decoders are deselected (no selected outputs) when one or both chip enables are inactive, putting all test inverters in a known biased condition. Two of the quadrants have the test inverter inputs I_* connected to D as shown in Fig. 6 while the other two quadrants have inputs I_* connected to U.

Fig. 7 is an equivalent circuit of an enabled inverter matrix and the support electronics used to obtain measurements. The RRELAX inverter matrix measurements use a 12-bit Analog-to-Digital Converter (ADC). The inverter output voltage is measured when the output switch is in the V position and the current through the inverter (IDD) is measured when the output switch is in the I position. OP-amps OP1 and OP2 function as a current-to-voltage converter which holds the LO point at a virtual ground. AI 1 current measurements are corrected by a baseline leakage measurement made on the matrix when it is deselected. When the matrix is deselected, the matrix baseline leakage current is the sum of leakage currents through 32 off n-FETs and 32 off p-FETs.

When TIE is low the Digital-to-Analog (DAC) drives the inverter input and allows the measurement of inverter transfer characteristics. The data analyzed in this paper was all obtained with TIE high, where the internal feedback connection is made, bring the circuit to the inverter threshold condition.

DISCUSSION

Representative ground test results from the inverter matrix, shown in Figs. 8 to 10, were obtained from the Clementine spacecraft. Test results, shown in Figs. 11 to 13, were obtained from the Inter-Stage Adapter (ISA). The first results, shown in these figures, were obtained at JPL (Pasadena, CA) using an hp 4062 parametric tester to measure inverter matrix packages. Subsequent results were obtained from the inverter matrices mounted in the RRELAX. The second results were also obtained at JPL where the RRELAX was in a noise free environment. The third and fourth results were obtained with one RRELAX unit integrated into the Clementine spacecraft and the other RRELAX unit integrated into the Inter-Stage Adapter. The third result came from NRL (Naval Research aboratory, Washington DC); and the fourth

" result came from VAB Vandenberg Air Force Base, Lompoc, CA).

The symbols used in Figs 8 to 13 are explained in Table 4. The symbols indicate (a) the bias on the inverter gates during irradiation and (b) the amount of shielding. Thus test results are expected to diverge into four trends once the devices receive sufficient radiation.

The results shown in Fig. 8 to 13 indicate that the laboratory results have least variability. On occasion results from RRELAX can be noisy. The source of the noise is under investigation.

The measurement has the interesting attribute that it requires only a single input voltage namely VDD and the output is an easily measured voltage that ranges between the VTn and VDD - VTp. This makes the measurement extremely simple and robust. These are the kind of attributes needed in the noisy environment of a spacecraft.

CONCLUS1ON

The inverter matrix developed for the RRELAX meets the design goal of providing FET parameters from a lean data set. The quality of the data could be improved by designing the inverter matrix FETs with geometries closer to the VT extraction points. This is important because it would reduce the uncertainties in the data extraction process and provide parameters with less variations.

The noise encountered in the RRELAX is due to the spacecraft operating environment. The noise enters through the power supplied to the RRELAX. Also the RRELAX experimental devices are lightly shielded to allow a maximun exposure to radiation. This allows RF from spacecraft operations to be picked up by the RRELAX electronics. Hopefully, these noise sources will be small enough so that radiation effects will be clearly observed in the data.

ACKNOWLEDGMENTS

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3. N. Weste and K. Eshraghian, Principles of CMOS VLSI Design, A systems Perspective, Addison-Wesley (Reading, MA, 1985).

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Table 1. Inverter matrix inverter geometries

DIMENSIONS (μm)			
Wp	Lp	Wn	Ln
7.2	1.2	9.6	1.2
28.8	1.2	2.4	2.4
28.8	1.2	2.4	1.2
28.8	1.2	9.6	1.2
7.2	2.4	2.4	1.2
7.2	2.4	9.6	1.2
7.2	1.2	2.4	2.4
7.2	1.2	2.4	1.2
2.4	2.4	12.0	1.2
14.4	1.2	2.4	-2.4
12.0	1.2	2.4	2.4
7.2	2.4	2.4	2.4
2.4	3.3	2.4	1.5
1.8	2.4	2.4	1.2
19.2	2.4	19.2	2.4
2.4	2.4	14.4	1.2

"able 2. Inverter matrix test results (CZ071vab1) 'or the data shown in Fig. 5 and from MOSIS.

PARAM	UNITS	--- RRELAX ---		--- MOSIS ----	
		n-FET	p-FET	n-FET	p-FET
DL	μm	0.470	0.686	0.227	0.116
DW	μm	0.616	0.768	0.524	0.620
VT	V	0.690	0.952	0.728	0.903
θL	μm/ L	0.136	0.118	---	---
KP	μA/V^2	65.324	20.160	86.400	26.600
CC	--	0.998	0.995	---	---

A

Table 3.   FET Dimensions for the curves shown in Fig. 5.

CURVE	$W(\mu m)$	$L(\mu m)$
#1	7.2	2.4
#2	7.2	1.2
#3	28.8	1.2
#4	2.4	2.4
#5	2.4	1.2
#6	9.6	1.2

Table 4.   Symbols for Figs. 8 to 13.

DEVICE	SHIELD mil Al	GATE-HIGH-BIAS QUAD#1 QUAD#3	GATE-LOW-BIAS QUAD#2 QUAD#4
Z07-INVT12	37	SQUARE	PLUS (+)
Z08-INVT11	7	DIAMOND	CROSS (X)

Figure 5.   Inverter matrix data analysis showing the nine cardinal points (squares) and six bonus points (triangles). (CZ071vab1)

Figure 3.   Spatial dependence of the inverter threshold voltage.
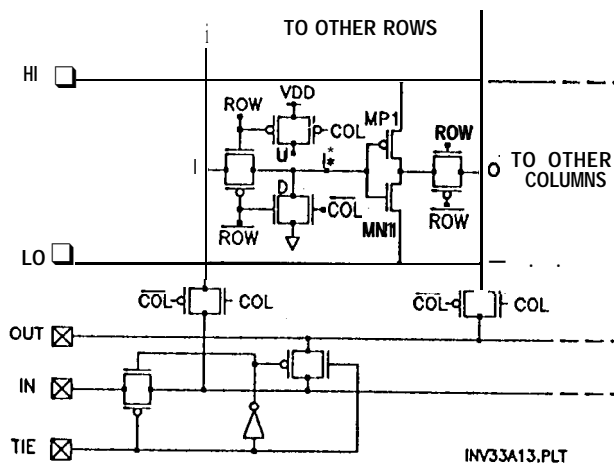
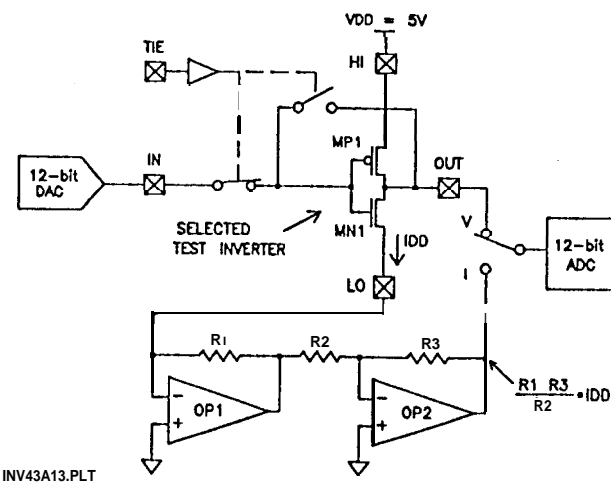Figure 6.   Inverter matrix circuit diagram showing one test inverter (MN1 and MP1) and signal steering transistors.
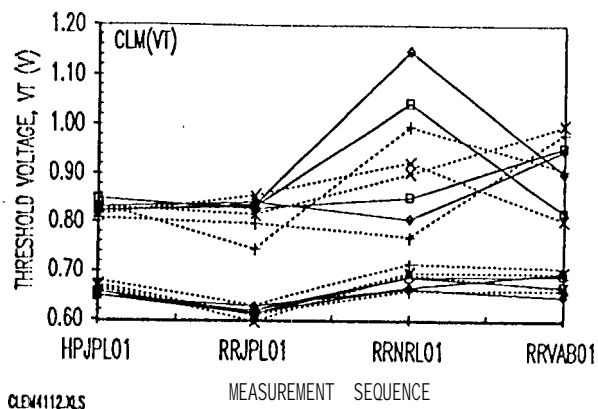

Figure 4.   Inverter matrix transfer curves for one of the four quadrants.

Figure 7.   Test inverter measurement circuitry.

Figure 8.   **Clementine** VT wi th VT$_n$ below and **VT$_p$** above.
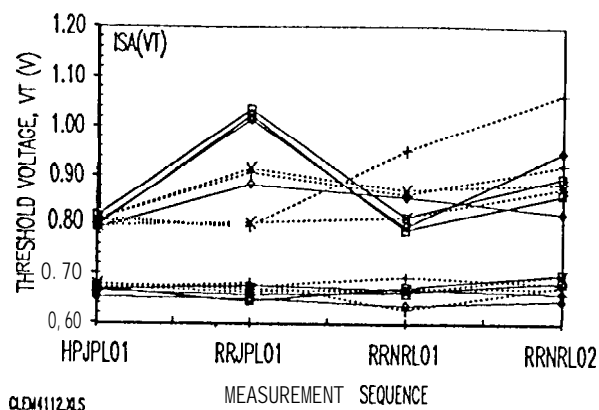

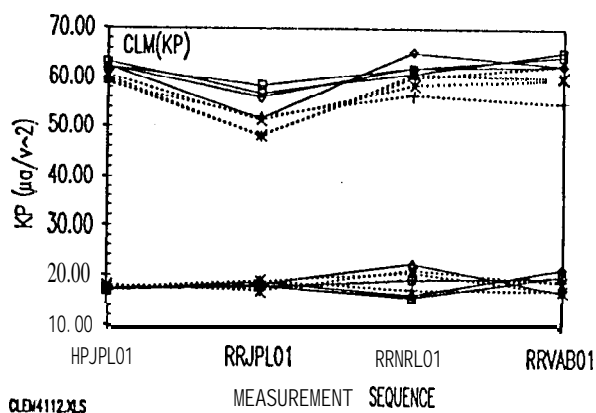
Figure 11.   ISA **VT with VT$_n$ below and VT$_p$** above.

Figure 9.   **Clementine** KP wi th KP$_n$ above **and KP$_p$ below.**
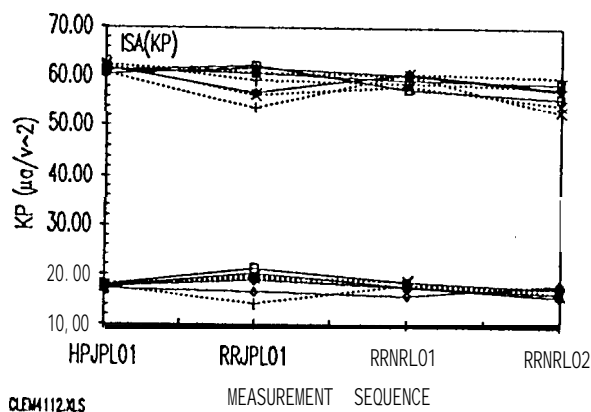
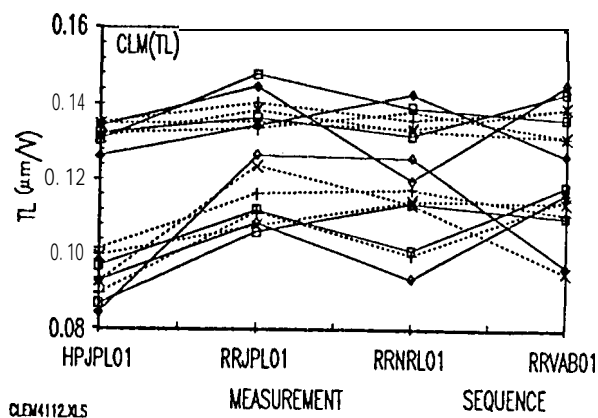Figure 12.   I SA KP wi th KP$_n$ above and **KP$_p$ below.**

Figure 10,   **Clementine** TL = θL with TL$_n$. θL_n above and **TL$_p$ = θL_p below.**
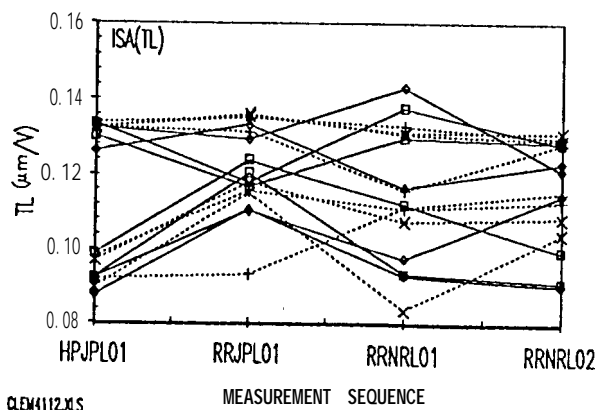

Figure 13.   I SA TL = θL wi th T L$_n$ = θL_n above and **TL$_p$** = θL_p below.

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